28.4 A 20Gb/s Bidirectional Transceiver Using a Resistor-Transconductor Hybrid

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This paper presents a 20Gb/s simultaneous bidirectional transceiver using a resistor-transconductor (*R-gm*) hybrid in standard 0.11µm CMOS.

As the performance of CMOS ICs dramatically improves, demands for I/O bandwidth increase substantially. In links in which signal transfer takes place in both directions (e.g., interprocessor links in multi-processor servers), simultaneous bidirectional signaling is attractive since it doubles the date rate per pin. The key component required for bidirectional signaling is a hybrid circuit that extracts the inbound signal from the signal line. For a data rate greater than 2.5Gb/s per direction [1], a replica driver was used to generate the outbound signal that should be subtracted from the signal on the transmission line. However, the mismatch between the replica and main driver and the settling time of the sampler limited the maximum bandwidth to 8Gb/s.

The simultaneous bidirectional transceiver we fabricated consists of a transmitter, a receiver and a hybrid circuit (Fig. 28.4.1). The transmitter launches a 10Gb/s serial signal onto a balanced line through the voltage divider in the hybrid. The divider serves as a termination resistor for the inbound signal. The input signals of the hybrid are the receiving-end voltage V and the current sensing voltage V_s obtained from the voltage divider. The hybrid extracts the inbound signal from these signals, and passes the resulting signal to the receiver front end. It works in the continuous-time domain, without using a replica driver or clock signals. This makes the design of the proposed hybrid much easier than a conventional hybrid, which requires precise matching between the main and the replica drivers in terms of delay, frequency response and gain.

The principles of a conventional hybrid using a replica driver [1] and our *R-gm* hybrid are shown in Fig. 28.4.2. The signal voltage on the line, V, is a superposition of the outbound-voltage wave V_f and the inbound-voltage wave V_r; hence, $V = V_f + V_r$. The conventional hybrid produces the inbound signal V_r by subtracting V_f from V ($= V_f + V_r$) by using a subtractor that uses the value of V_f generated by a replica driver (Fig. 28.4.2(a)). Our method is equivalent to subtracting Z_0I ($= V_f - V_r$) from V, where Z_0 is the impedance of the transmission line and I is the current flowing on the line. This also produces a signal proportional to V_r because $V - Z_0I = V - (V_f - V_r) = 2V_r$. To sense the current on the transmission line, we split the termination resistor into two parts, a current-sensing resistor, r, and the rest of the resistor, $Z_0 - r$, forming a voltage divider. The voltage at the node connecting these two parts, V_s, is used to sense the current. Because $I = (V_s - V)/r$, we obtain $V - Z_0I = (1 + Z_0/r)V - (Z_0/r)V_s$, which means that a weighted sum of V and V_s generates the inbound signal V_r. The weighted sum is produced by transconductors sharing a resistive load. Note that the data paths in the hybrid are differential, though the single-ended representation is used in Figs. 28.4.1 and 28.4.2.

As shown in Fig. 28.4.3, we used a simple NMOS differential pair for the transconductors because of their high-speed operation. The two inputs of the transconductors are connected to the complementary signal nodes to eliminate common-mode noise on the line. The current-sensing resistor, r, is set to $Z_0/2$; thus the transconductors sensing V and V_s have a transconductance ratio of $(1+Z_0/r):(Z_0/r)=3:2$.

Variations in the values of r and Z_0 reduce the attenuation of the outbound signal going into the receiver. To compensate for the summing-weight error due to variations in r and Z_0, we adjust the tail current of the transconductor that senses V by controlling the external current I_{CN}. The weights are adjusted so that outbound signal is completely suppressed from the hybrid output at dc. To minimize the remaining high-frequency signal leakage from the outbound signal, the frequency responses of the signal paths from the inputs V and V_s to the output should be matched. Since the two transconductors share a load, the difference in the high-frequency responses comes from the input RC time constants, which can be adjusted by inserting a PMOS resistor in the input signal path of the transconductor sensing V_s. In this implementation, an external control voltage V_{CP} is applied to the gate of the PMOS to adjust the resistor value.

The transfer functions of the *R-gm* hybrid simulated using SPICE are shown in Fig. 28.4.4. When a signal is sent from the transmitter at the other end of the line, the insertion loss of the hybrid is less than 5dB from dc to 10GHz. When a signal originates from the internal transmitter, the signal transfer, or leakage from the internal transmitter, is 40dB below that of the inbound signal from dc to 5GHz. Figure 28.4.5 shows the SPICE simulated transient waveforms of a 20Gb/s bidirectional transmission. The error voltage in the hybrid output due to the outbound signal, V_{Error}, is suppressed as low as 1mV.

In the bidirectional transceiver, we reused an existing 10Gb/s transceiver [2]. The transmitter consists of a PRBS generator that produces 2^{23}-1 patterns, 64:1 multiplexers, and the main and auxiliary output buffers. The transmitter has a data path to feed 1-bit delayed data to the auxiliary output buffer to compensate for up to 5dB of the high-frequency signal loss. The receiver [3] consists of an equalizer, decision latches and following demultiplexers that perform 1-to-32 serial-parallel conversion, and a CDR circuit. Two data paths that sample the equalizer output at the centers and boundaries of the bit cells are used to perform the 2× oversampling clock recovery.

The test chip was fabricated in 0.11µm CMOS technology. A micrograph and summary of performance are shown in Fig. 28.4.7. The areas of the transmitter and receiver were 0.9×0.53mm² and 0.45×1.2mm². The area overhead for bidirectional signaling was 0.035×0.055mm², or 0.2% of the total area. The power consumptions of the transmitter and receiver, including the *R-gm* hybrid, were 126 and 130mW respectively. The power overhead of the bidirectional signaling was 7mW, or 3% of the total power.

Figure 28.4.6 shows an eye diagram observed at the chip I/O pin and a bathtub curve of the receiver with a channel loss of 5dB when 20Gb/s bidirectional signaling was performed. The receiver bathtub curve was measured by disabling the CDR circuit and changing the transmitter clock phase with reference to the receiver clock phase. The timing margin that guarantees a BER less than 10^{-12} was 58ps.

References:

[1] A. Martin et al., "8Gb/s Differential Simultaneous Bidirectional Link with 4mV 9ps Waveform Capture Diagnostic Capability," *ISSCC Dig. Tech. Papers*, pp. 78-79, Feb., 2003.
[2] H. Takauchi et al., "A CMOS Multi-Channel 10Gb/s Transceiver," *ISSCC Dig Tech. Papers*, pp. 72-73, Feb., 2003.
[3] Y. Tomita et al., "A 10Gb/s Receiver With Series Equalizer and On-chip ISI Monitor in 0.11µm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 986-993, Apr., 2005.

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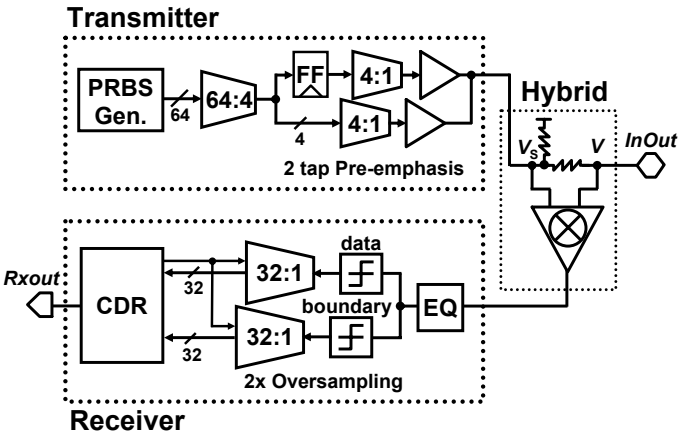

Figure 28.4.1: Block diagram of transceiver.

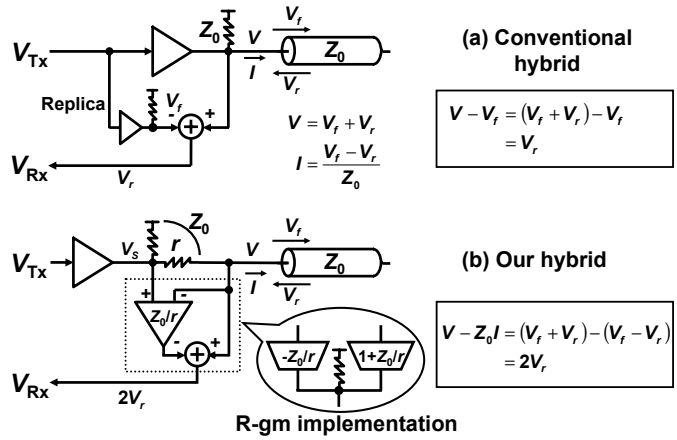

Figure 28.4.2: Hybrid circuit, (a)Replica hybrid (conventional), and (b)Our R-gm hybrid.

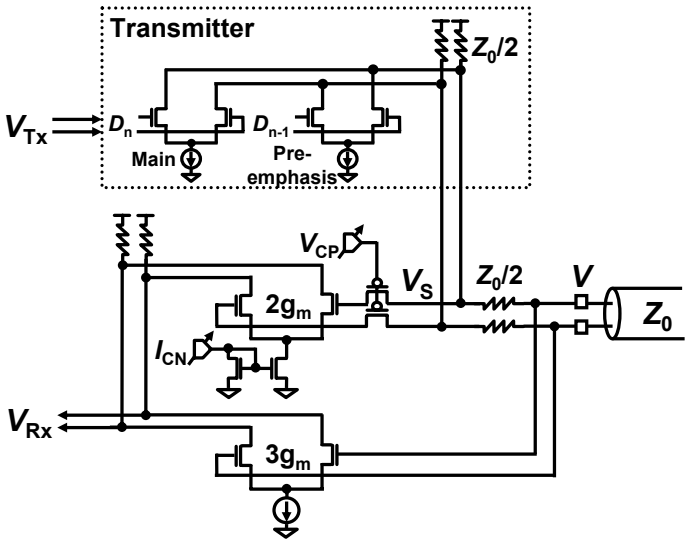

Figure 28.4.3: Differential circuit implementation of R-gm hybrid (from Fig. 28.4.2 (b)).

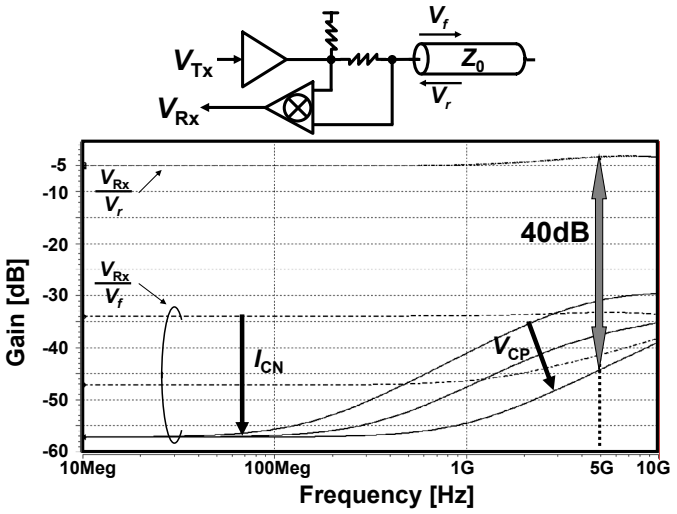

Figure 28.4.4: Transfer functions of R-gm hybrid simulated by SPICE.

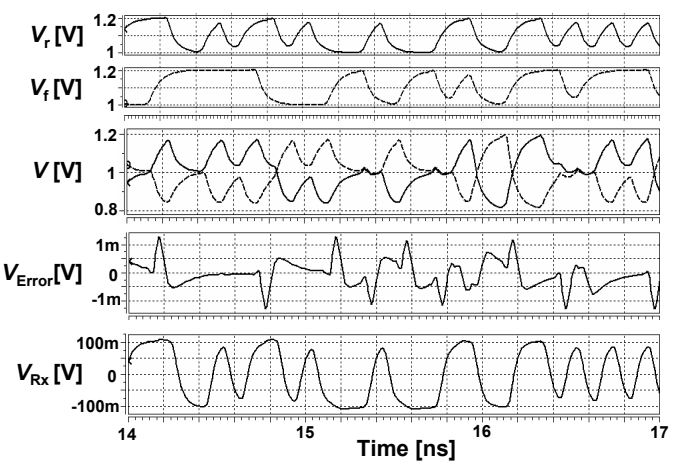

Figure 28.4.5: R-gm hybrid bi-directional signaling operation.

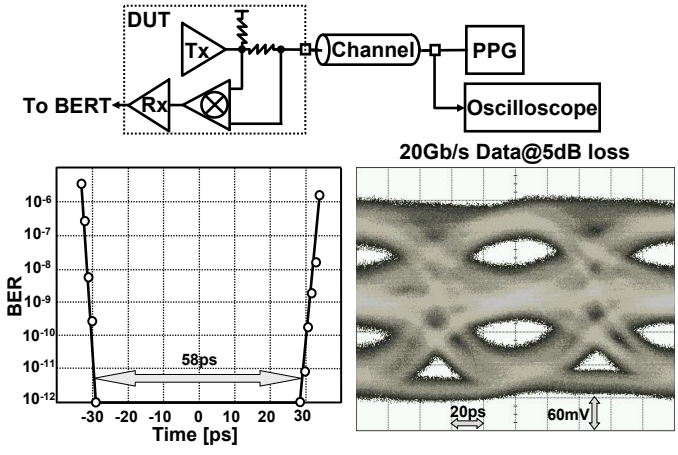

Figure 28.4.6: Measured eye pattern and bathtub curve.

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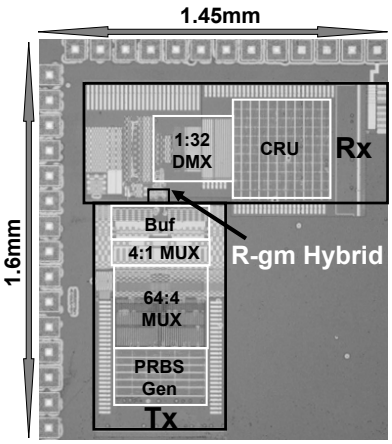

Summary

Data rate	20Gb/s (bidirectional)
Supply voltage	1.2V
Technology	0.11μm CMOS
Power	
Tx	126mW
Rx	130mW
Hybrid	7mW
Area	
Tx	0.9x0.53mm^2
Rx	0.45x1.2mm^2
Hybrid	0.035x0.055mm^2

Figure 28.4.7: Micrograph and performance summary.

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